REMARKS

Claims 1-15, and 17-21 are pending. Claims 1, 7, 11, 13, 14 and 15 are amended. Claim 16 is canceled. Claims 1-15 and 17-21 stand rejected.

Interview Summary

Applicant's representative wishes to thank Examiner Thomas and Primary Examiner Vikkram Bali for taking the time to conduct a telephonic interview on December 7, 2007. During the interview, the Applicant's representative presented proposed comments to clarify the claim features of claim 1 and how these features were not met by the Chow and Whitted references. Examiner Thomas provided a discussion of the claim structure and how the Whitted reference was interpreted from the Examiner's point of view. No agreement was reached, although the Examiner indicated that she would further consider this written response.

Regarding the Rejections under 35 U.S.C. §103

Claims 1-15 and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow et al (US 6,292,589) in view of Whitted et al, "A software Testbed for the Development of 3D Raster Graphics Systems" (January 1982, ACM Transactions on Graphics, New York, NY, USA Volume 1, Issue 1, Pages 43-58, hereafter Whitted). These rejections are respectfully traversed.

Regarding claims 1, 7, 11, 13 and 15, the claims have each been amended to recite "processing each block within at least one shader module" to further distinguish the instant invention from the cited references. These amendments are fully supported in paragraphs [0028], [0036], and [0037] of the specification. In addition, each of the independent claims recites the specific processing features that occur within the shader module. For example, claim 1 recites that "wherein said multiplying a column or row of pixels with a predetermined matrix to generate a corresponding set of output pixels, determining, and sampling the pixels are performed by said at least one shader module," claim 7 recites that "said creating a polyline and creating a line are performed by said at least one shader module," claim 11 recites that "said multiplying and adding are performed by said at least one shader module",

and claim 13 recites that "for each column in a block of pixels, setting up a shader and rendering a scanline, and for each row in a block of pixels, setting up a shader and rendering a column, and wherein the setting up and the rendering are performed by said at least one shader module." Additionally, Claim 15 recites "for each set of scanlines, sampling the pixels comprised within the scanlines and multiplying the sampled pixels with a row or column of the predetermined matrix, and wherein said setting up and the rendering are performed by said at least one shader module". The Office Action admits that the Chow et al reference does not teach calculation or pixel manipulation within a shader module and looks to the Whitted reference to remedy this lack. The Office Action appears to assert that the Whitted reference teaches or discloses these features in Figure 1, page 44, however, it does not.

The instant invention recites a shader module used in association with a discrete cosine transformation (DCT) algorithm to process incoming 8x8 blocks of pixels by forming a cross product with an orthogonal matrix to preserve the values of the incoming pixels quickly in block and matrix dot product sets. These sets are preserved as textured lines and scanlines and stored into memory quickly, thus eliminating pixel loss. The input video data capture process is therefore greatly enhanced. To process this incoming data prior to delivery to a CPU or an output process, a shader module is employed using the correct matrix values and array offsets to allow DCT processing of each group of textured lines and scanlines as parallel processes. This process improves not only data capture but also improves processing speed for all pixels within the captured video data.

The recitations in the claims are not simply in reference to a shader, but to what processing is occurring within the shader as a part of the overall process. Claim 1, for example, recites "processing each block within at least one shader module" and where "said multiplying a column or row of pixels with a predetermined matrix to generate a corresponding set of output pixels, determining, and sampling the pixels are performed by said at least one shader module", which details the offloading of the CPU by performing these actions by a shader module within the GPU. The Office Action seems to assert that the inclusion of a shader function within figure 1 of the Whitted reference teaches that these functions are performed by the shader function disclosed in that figure, however, it does not.

The Whitted reference includes a shader function that performs an interpolation of intensity values for pixels processed using a z-buffer to determine visibility (page 48, last paragraph). This is not the same as performing matrix operations such as multiplying and sampling as recited in the claims. The Whitted reference further discloses on page 51, third full paragraph, that operations are performed by other arithmetic modules in order to minimize "the number of unnecessary operations performed by the shader". In Whitted, the shader is reserved for the final display stage in order to determine pixel intensity values only (page 48, last full paragraph and page 51, first full paragraph). There is no disclosure or teaching for a shader module within a GPU performing matrix operations such as "multiplying a column or row of pixels with a predetermined matrix to generate a corresponding set of output pixels, determining, and sampling the pixels" as recited in the submitted claim 1.

The Whitted reference similarly does not teach or disclose "said creating a polyline and creating a line are performed by said at least one shader module," as recited in claim 7, "said multiplying and adding are performed by said at least one shader module" as recited in claim 11, "setting up a shader and rendering a scanline, and for each row in a block of pixels, setting up a shader and rendering a column, and wherein the setting up and the rendering are performed by said at least one shader module" as recited in claim 13, or "wherein said setting up and the rendering are performed by said at least one shader module" as recited in claim 15. Again, the shader disclosed in the Whitted reference is used for pixel intensity interpolation in the final stage of graphics processing (fig 1, and page 48, last paragraph) and does not disclose or teach performing the above functions as recited in claims 7, 11, 13 and 15.

Therefore, the combination of Chow et al, and Whitted fails to provide the teachings needed to establish that claims 1, 7, 11, 13 and 15 are obvious. These claims are allowable for at least the reasons given above. Accordingly, reconsideration and allowance are respectfully requested.

Regarding claims 2-6, 8-10, 12, 14-15, and 17-21, these claims each depend from one of independent claims 1, 7, 11, 13 or 15. In view of the above, it is clear that the combination of Chow et al and Whitted fails to provide the teachings to establish that claims 1, 7, 11, 13 and 15 are obvious. The dependant claims are, therefore, allowable for at least the reasons

shown for claims 1, 7, 11, 13 and 15. Accordingly, reconsideration and allowance are respectfully requested.

CONCLUSION

For the foregoing reasons, Applicants respectfully submit that the instant application is in condition for allowance.

Respectfully submitted,

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